The Total Ionizing Dose Performance of Deep Submicron CMOS Processes

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Aerospace & Defense

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Special Thanks

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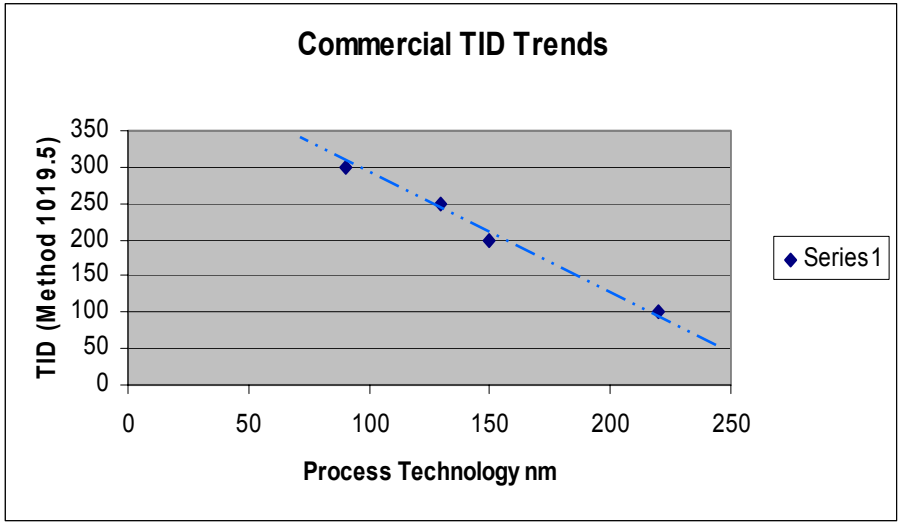
- TID exposure and evaluations were jointly conducted at NASA/GSFC under separate NASA funding by teams headed by Mike Xapsos and Dr. James W. Howard Jr.

History of Xilinx TID testing of Virtex commercial offerings

- **Virtex**
  - 220 nm CMOS technology with 6 metal layers
  - Method 1019.5 specification achieved 100 krads(Si) at space dose rates
- **Virtex II**
  - 150 nm CMOS technology with 7 metal layers
  - Method 1019.5 specification achieved 200 krads(Si) at full 1019 dose rate
- **Virtex II-Pro**
  - 130 nm CMOS technology with 8 metal layers
  - Method 1019.5 specification demonstrated 250 krads(Si) at full 1019 dose rate
- **Virtex 4**
  - 90 nm CMOS technology with 10 metal layers
  - Method 1019.5 specification demonstrated 300 krads(Si) at full 1019 dose rate
- **Virtex 5**
  - 65 nm CMOS technology with 11 metal layers
  - Initial tests ongoing
  - Transistor level data suggests value north of 500 krads(Si) may be achievable at full 1019 dose rate



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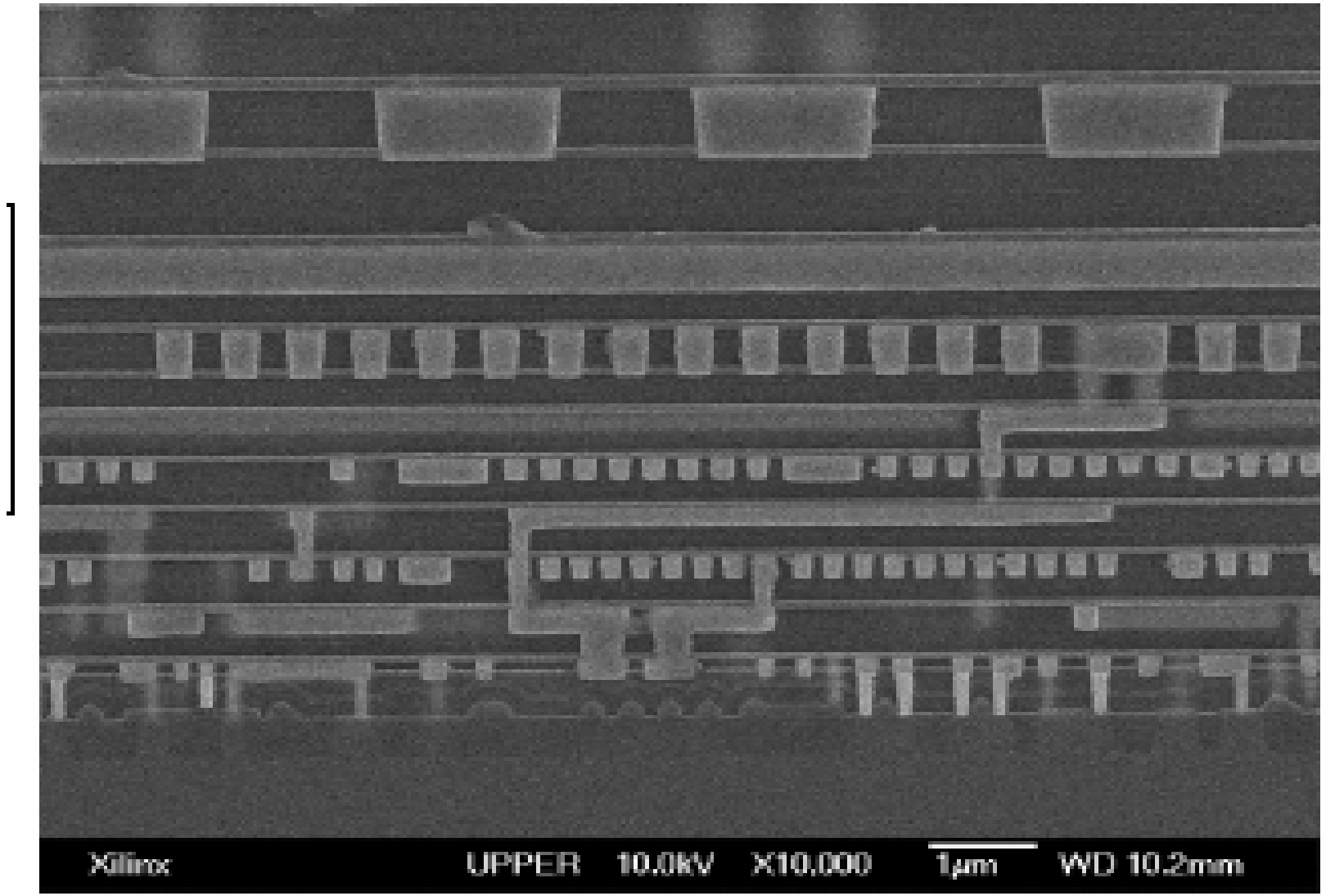
Technologies Evaluated

Virtex 4 (90 nm CMOS) 1st generation triple-oxide

- Lightly doped P-silicon 3.0µm epitaxial substrate
- Heavily doped P-silicon “handle” wafer
- Shallow Trench Isolation
- Three discreet transistor structures
  - Gate oxide targets of 22.5A, 29.5A and 62.0A
- 10 layers of metallization
  - 10 Copper plus one Aluminum pad metallization
- Full dual damascene copper process (no via plugs)

90 nm Typical Cross Section



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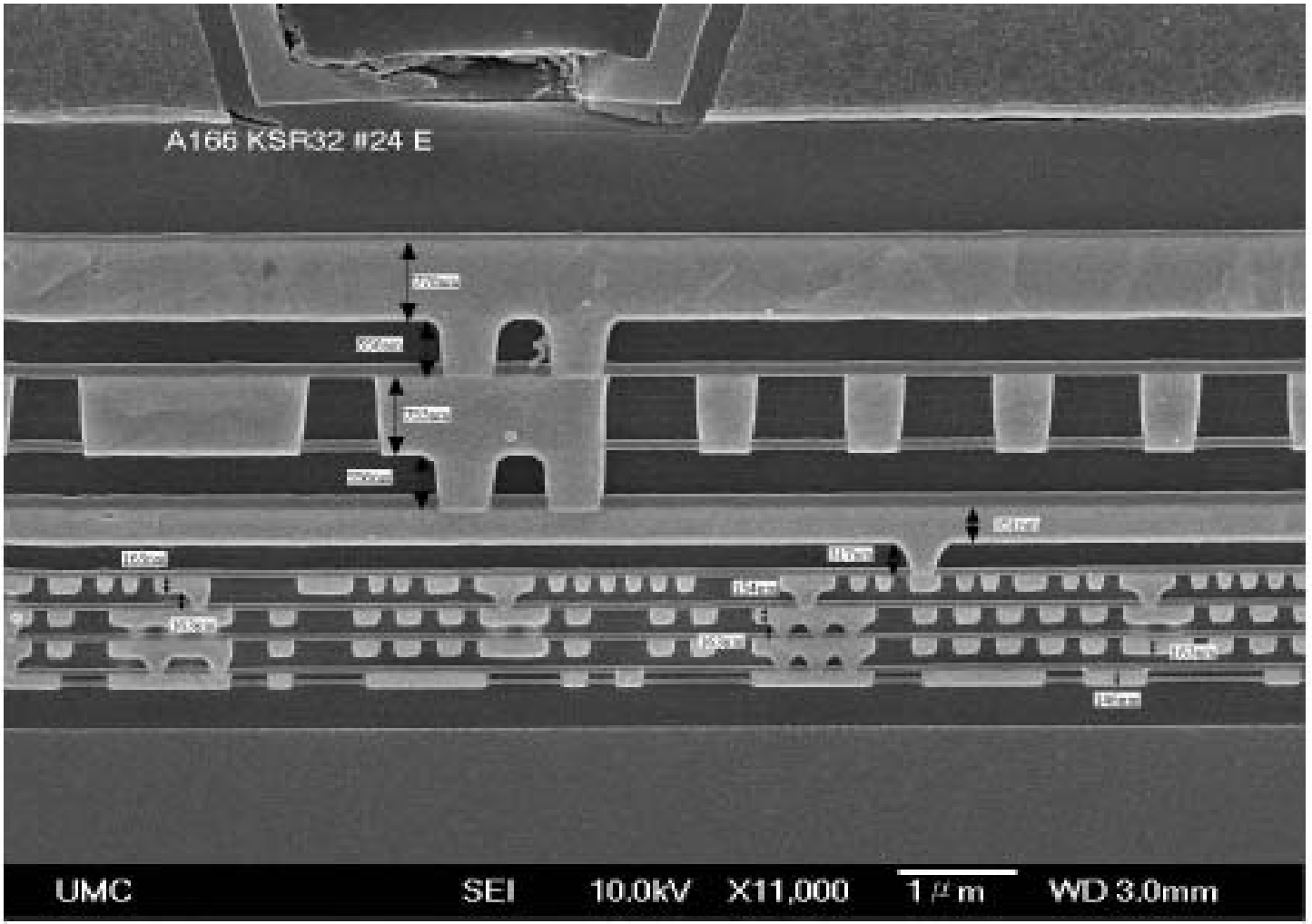
Technologies Evaluated

Virtex 5 (65 nm CMOS) 2nd generation triple-oxide

- Lightly doped P-silicon 2.0µm epitaxial substrate
- Heavily doped P-silicon “handle” wafer
- Shallow Trench Isolation
- Three discreet transistor structures
  - Gate oxide targets of 14.8A, 23.5A and 63.0A
- 11 layers of metallization
  - 11 Copper plus one Aluminum pad metallization
- Full dual damascene copper process (no via plugs)

65 nm Typical Cross Section



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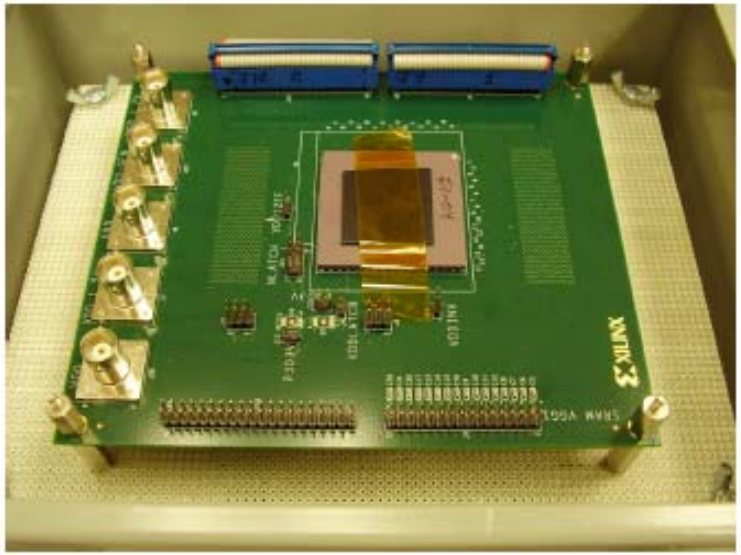
Co60 Testing of 90 and 65* nm transistor structures at GSFC

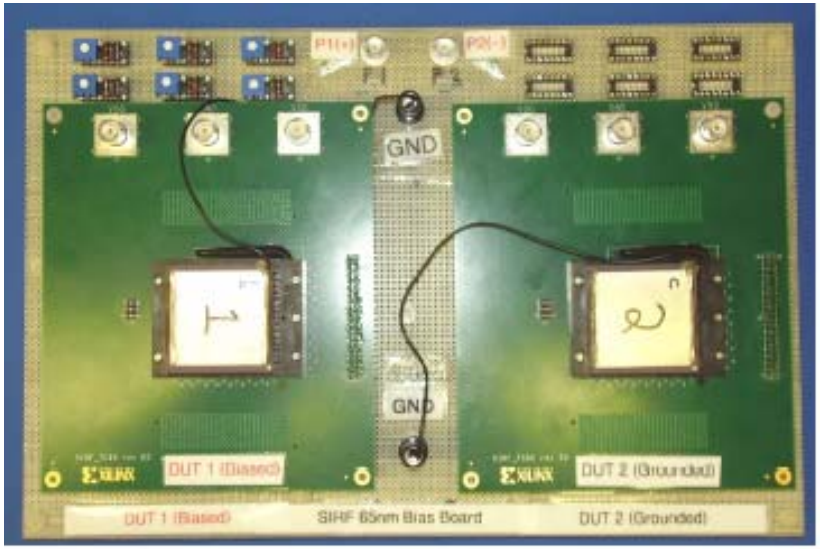
- Selected test transistors from the SIRF 90nm and 65 nm test chips were irradiated at various dose rates at the GSFC Co-60 facility
- Transistor samples of both technologies were irradiated with “on bias” and “off bias” to TID levels well in excess of 1800 krads(Si)
- TID results on the 90 nm structures were reported in the NASA Test Results Publication dated 12 October 2006 (copies are available)
- TID results on the 65 nm structures were reported in the NASA Test Results Publication dated 25 January 2008 (copies are available)
- Test results for both technologies were fully compatible with the SIRF TID program goals (as noted in the abstracts below, taken from the NASA reports)
- NASA assessment of the 90 nm technology was “*the basic conclusion of this testing is that the radiation tolerance of these transistor technologies is sufficient to withstand Mrad(Si) doses with only minor IV characteristic changes”.*
- NASA assessment of the 65 nm technology was that *“the test data can best be summarized by stating that the SIRF 65 nm transistors can withstand total doses well in excess of 1 Mrad(Si)”*

*

NASA Co-60 Test Fixtures



Test PCB and 90 nm test device with a taped lid (to protect the bond wires.



Bias board with 2 mounted 65 nm test boards containing packaged chips used for Co-60 gamma ray irradiations

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Biases used for 65 nm parts

NMOS thin	+1.0 V
NMOS mid	+1.5 V
NMOS thick	+2.5 V
PMOS thin	-1.0 V
PMOS mid	-1.5 V
PMOS thick	-2.5 V

Bias during irradiation

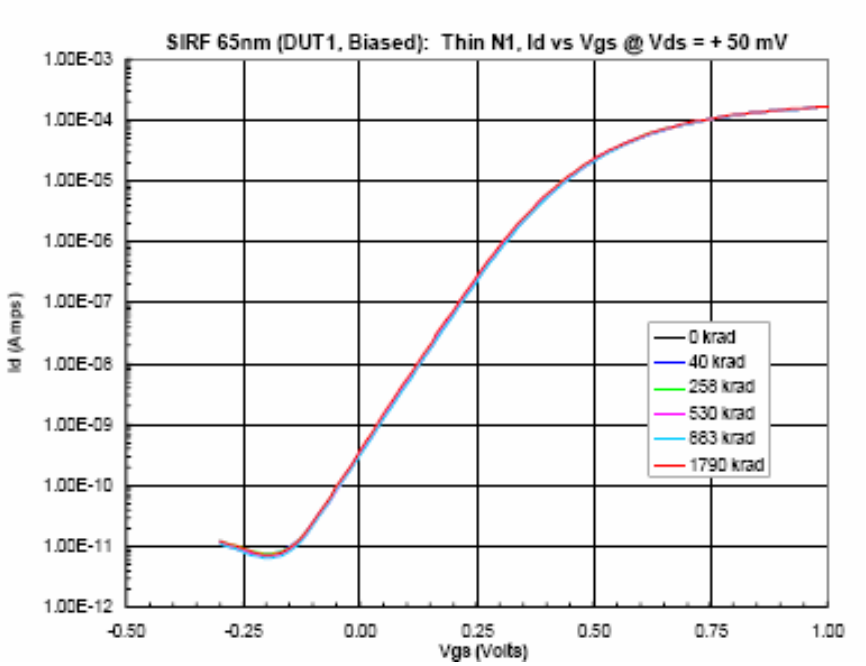
Transistor Type:	Measurement:	V_{gs} Sweep:	V_{ds} Values:
NMOS thin	I_d vs. V_{gs}	-0.3 to +1.0 V	+0.05, +1.0 V
NMOS mid	I_d vs. V_{gs}	-0.4 to +1.5 V	+0.05, +1.5 V
NMOS thick	I_d vs. V_{gs}	-0.5 to + 2.5 V	+0.05, +2.5 V
PMOS thin	I_d vs. V_{gs}	-1.0 to +0.3 V	-0.05, -1.0 V
PMOS mid	I_d vs. V_{gs}	-1.5 to +0.4 V	-0.05, -1.5 V
PMOS thick	I_d vs. V_{gs}	-2.5 to + 0.5 V	-0.05, -2.5 V

Bias conditions for sub-threshold measurements

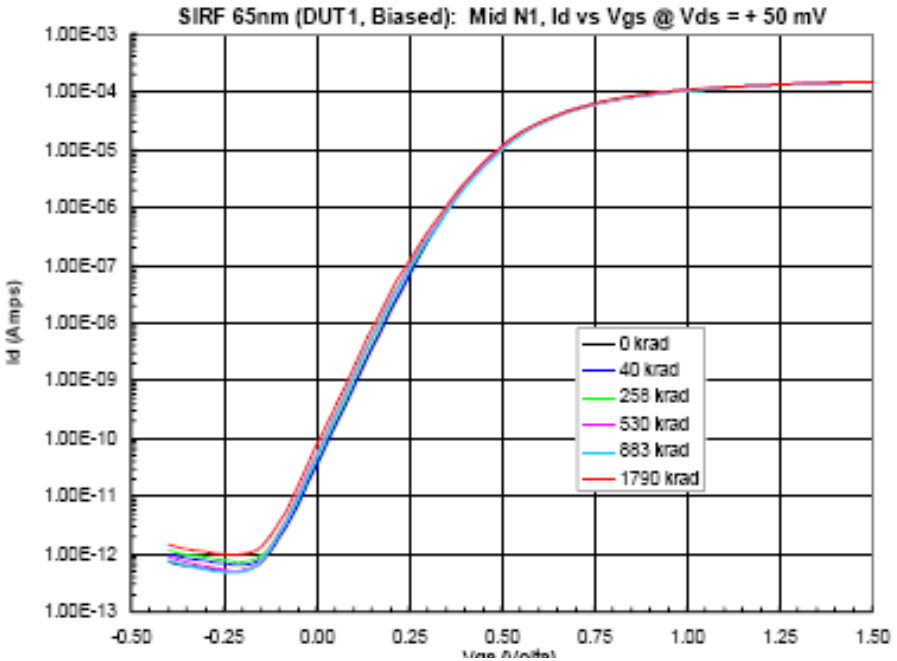
Transistor Type:	Measurement:	V_{ds} Sweep:	V_{gs} Values:
NMOS thin	I_d vs. V_{ds}	0 to +1.0 V	+0.4, +0.6, +0.8 V
NMOS mid	I_d vs. V_{ds}	0 to +1.5 V	+0.6, +0.9, +1.2 V
NMOS thick	I_d vs. V_{ds}	0 to +2.5 V	+1.0, +1.5, +2.0 V
PMOS thin	I_d vs. V_{ds}	0 to -1.0 V	-0.4, -0.6, -0.8 V
PMOS mid	I_d vs. V_{ds}	0 to -1.5 V	-0.6, -0.9, -1.2 V
PMOS thick	I_d vs. V_{ds}	0 to -2.5 V	-1.0, -1.5, -2.0 V

Bias conditions for forward char measurements

TID response of 65 nm N-transistors



Thin oxide transistor



Mid oxide transistor

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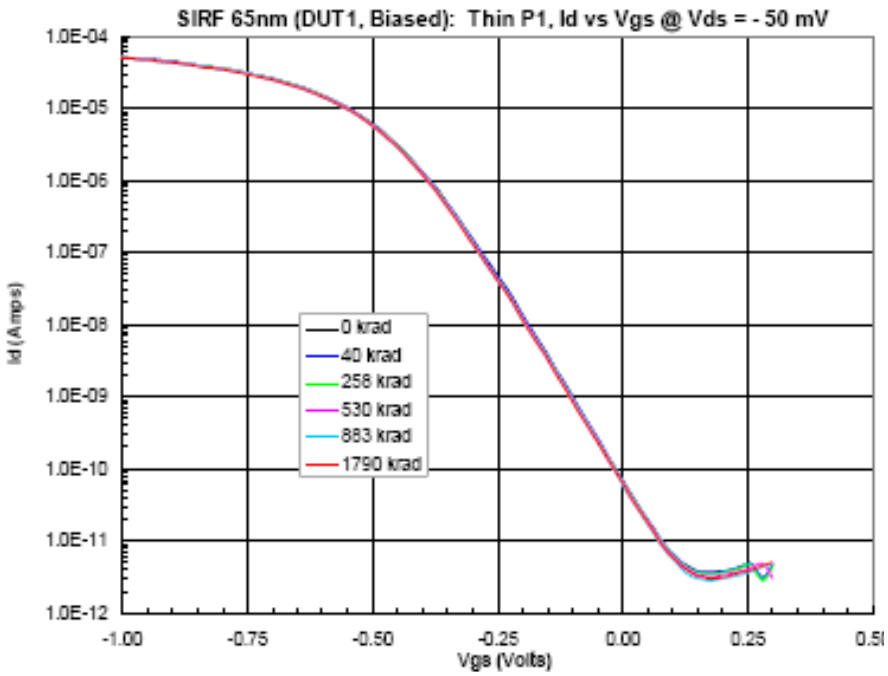
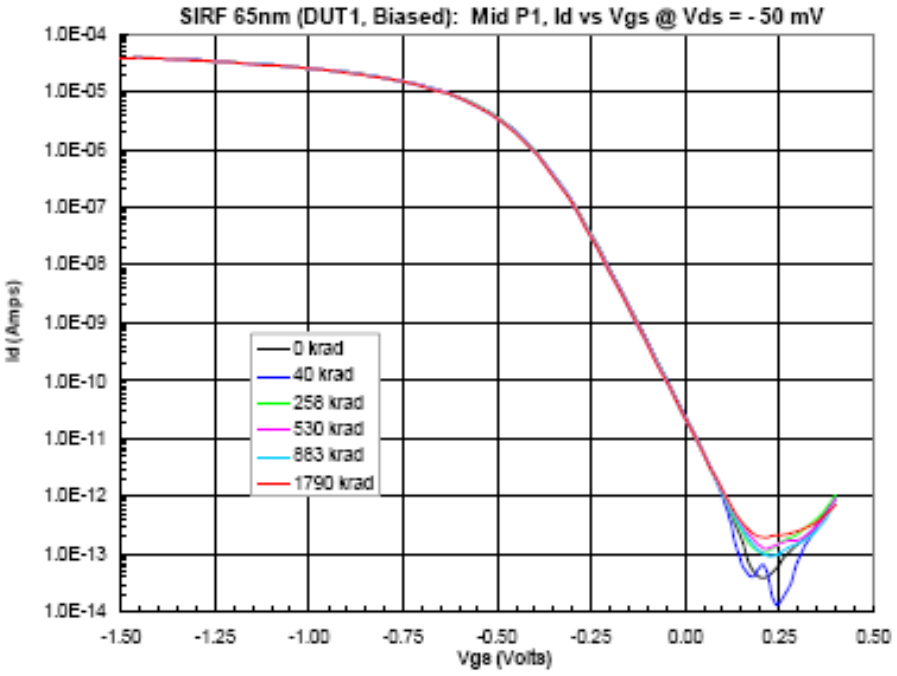
TID response of 65 nm P-transistors



Thin oxide transistor



Mid oxide transistor

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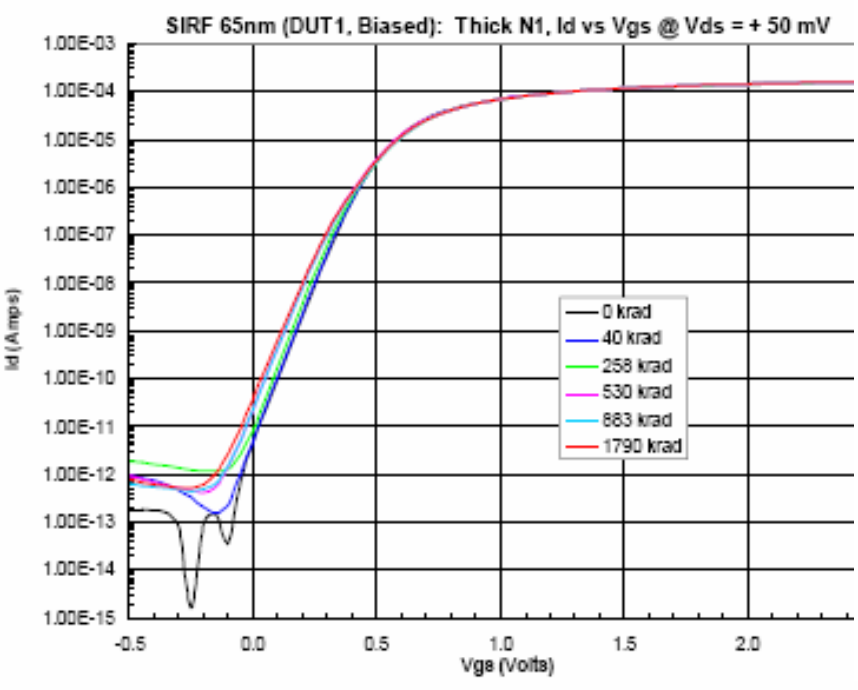
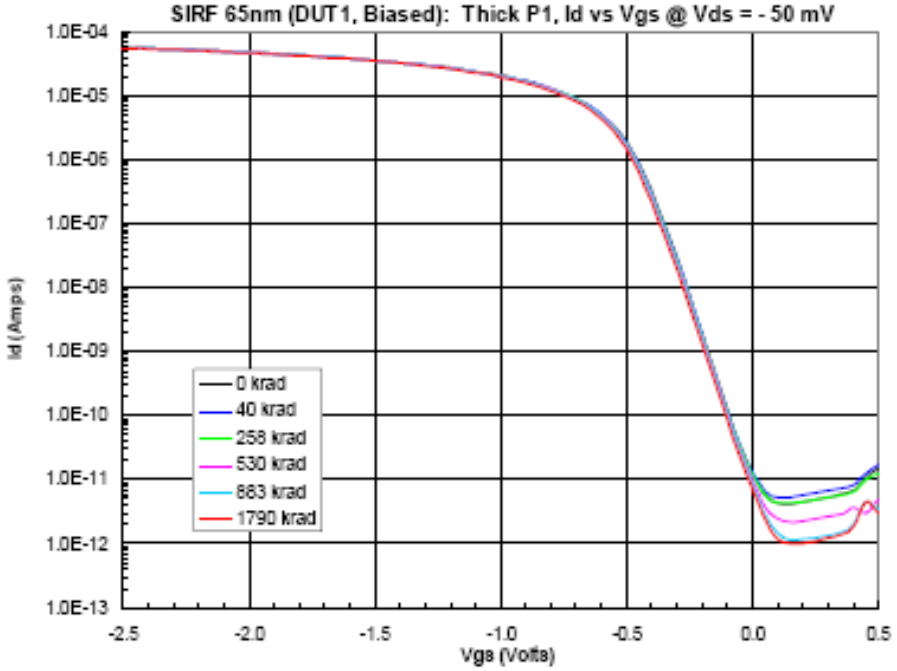
TID response of I/O transistors



Thick oxide N-type transistor



Thick oxide P-type transistor

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Parametric results for all transistors biased "on"

Transistor Information			Threshold Voltage (Volts)		Max Transconductance ($Ohms^{-1}$)		Subthreshold Swing (mV / decade)	
Oxide	Transistor	W/L	at 0 krad	at 1.79 Mrad	at 0 krad	at 1.79 Mrad	at 0 krad	at 1.79 Mrad
Thin	NMOS1	2.0/0.07	0.429	0.426	3.62E-04	3.62E-04	86.6	83.7
Thin	NMOS2	10x 0.2/0.07	0.356	0.350	3.02E-04	3.05E-04	77.8	78.6
Thin	NMOS3	2.0/2.0	0.409	0.405	1.82E-05	1.81E-05	86.8	87.3
Thin	PMOS1	2.0/0.07	-0.435	-0.436	1.07E-04	1.04E-04	86.6	88.6
Thin	PMOS2	10x 0.2/0.07	-0.401	-0.409	1.08E-04	1.02E-04	83.1	84.7
Thin	PMOS3	2.0/2.0	-0.338	-0.340	5.18E-06	5.12E-06	72.6	72.2
Mid	NMOS1	2.0/0.12	0.450	0.447	2.28E-04	2.26E-04	74.3	73.8
Mid	NMOS2	10x 0.25/0.12	0.387	0.371	2.41E-04	2.41E-04	74.5	77.5
Mid	NMOS3	2.0/2.0	0.316	0.312	1.88E-05	1.88E-05	71.3	70.9
Mid	PMOS1	2.0/0.15	-0.412	-0.415	4.85E-05	4.80E-05	78.1	79.7
Mid	PMOS2	10x 0.2/0.15	-0.380	-0.391	5.17E-05	4.98E-05	76.3	78.3
Mid	PMOS3	2.0/2.0	-0.307	-0.313	6.04E-06	6.02E-06	77.8	79.4
Thick	NMOS1	3.8/0.24	0.504	0.510	1.52E-04	1.51E-04	75.8	82.0
Thick	NMOS2	10x 0.38/0.24	0.424	0.382	1.58E-04	1.50E-04	78.6	89.6
Thick	NMOS3	3.8/3.8	0.569	0.579	9.44E-06	9.39E-06	71.1	79.7
Thick	PMOS1	3.8/0.24	-0.448	-0.466	3.97E-05	3.89E-05	85.3	86.6
Thick	PMOS2	10x 0.38/0.24	-0.430	-0.458	3.58E-05	3.44E-05	82.8	85.3
Thick	PMOS3	3.8/3.8	-0.469	-0.487	2.61E-06	2.59E-06	73.6	76.0

Parametric results for all transistors biased “off”

Transistor Information			Threshold Voltage (Volts)		Max Transconductance ($Ohms^{-1}$)		Subthreshold Swing (mV / decade)	
Oxide	Transistor	W/L	at 0 krad	at 1.79 Mrad	at 0 krad	at 1.79 Mrad	at 0 krad	at 1.79 Mrad
Thin	NMOS1	2.0/0.07	0.432	0.427	3.59E-04	3.64E-04	85.9	84.7
Thin	NMOS2	10x 0.2/0.07	0.369	0.355	3.17E-04	3.22E-04	77.5	76.8
Thin	NMOS3	2.0/2.0	0.413	0.408	1.82E-05	1.80E-05	68.3	66.9
Thin	PMOS1	2.0/0.07	-0.452	-0.456	1.02E-04	9.65E-05	83.7	84.4
Thin	PMOS2	10x 0.2/0.07	-0.409	-0.417	1.04E-04	9.88E-05	82.3	83.7
Thin	PMOS3	2.0/2.0	-0.342	-0.343	5.15E-06	5.12E-06	71.7	71.5
Mid	NMOS1	2.0/0.12	0.408	0.432	2.24E-04	2.23E-04	75.8	72.4
Mid	NMOS2	10x 0.25/0.12	0.360	0.370	2.42E-04	2.35E-04	75.8	74.3
Mid	NMOS3	2.0/2.0	0.291	0.308	1.93E-05	1.88E-05	71.1	69.6
Mid	PMOS1	2.0/0.15	-0.418	-0.417	4.88E-05	4.76E-05	79.1	76.8
Mid	PMOS2	10x 0.2/0.15	-0.380	-0.386	5.16E-05	4.99E-05	77.0	77.8
Mid	PMOS3	2.0/2.0	-0.296	-0.297	5.88E-06	5.82E-06	76.8	77.3
Thick	NMOS1	3.8/0.24	0.430	0.470	1.49E-04	1.47E-04	82.3	87.2
Thick	NMOS2	10x 0.38/0.24	0.353	0.388	1.53E-04	1.48E-04	81.7	81.4
Thick	NMOS3	3.8/3.8	0.448	0.502	9.47E-06	9.25E-06	80.5	75.8
Thick	PMOS1	3.8/0.24	-0.445	-0.458	4.03E-05	3.97E-05	85.3	87.6
Thick	PMOS2	10x 0.38/0.24	-0.420	-0.443	3.58E-05	3.47E-05	81.4	83.4
Thick	PMOS3	3.8/3.8	-0.486	-0.477	2.64E-06	2.81E-06	82.5	83.7

TID test results summary

- Both the 90 nm test transistors and the 65 nm test transistors appear capable of operating through TID stress well in excess of 1 Mrad(Si) with proper design margins
- Key point to remember is that of all the presented transistor radiation TID data was taken on conventional transistor layouts, not on circular devices and not on dog-bone devices
- Xilinx typically simulates the operation of logic devices out to the full corner lot values of +/- 2.5 sigma
- For the 65 nm test transistors, all transistors for all bias states fell post radiation within the corner lot values of +/- 1.0 sigma used for circuit simulation
- In other words, parametric shifts out beyond 1.0 Mrad(Si) are well within normally expected process spreads with proper design margins